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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,840	03/06/2002	Yasunao Katayama	JP920010049US1	8580

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	5

DATE MAILED: 08/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/091,840	Applicant(s) KATAYAMA ET AL.	
	Examiner James C Kerveros	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 are pending and are hereby presented for examination, in response to the present US Application filed 3/6/2002.

Drawings

2. The drawings are objected to because Figures 1-20 are designated as --Prior Art--, while the specification describes Figures 1-5 and 14 as prior art and Figures 6-13 and 15-20 as the present invention. Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 1-6 are objected to because of the following informalities: In the independent claim 1, line 4, the expression "a processor, said processor in turn comprising" should be changed to "a processor comprising". Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1, 7, 12 and 18 recite the limitation "the obtained digital signals" in the last paragraph of each claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cameron (US 6317858).

Regarding independent Claims 1, 7, 12, 18, and dependent Claims 2, 13, Cameron discloses an apparatus and method for decoding an algebraic-coded message including Reed-Solomon (RS) codes, in a decoder unit 2, FIG. 1, comprising:

An input unit (syndrome generator 3), for entering coded digital signals from a raw received signal R (x) 1 including Reed-Solomon (RS) codes in accordance with a number of interleaved of Reed-Solomon (RS) codes.

A processor (polynomial solver 6) comprising error location polynomial calculator [L (x) 7] and error value polynomial calculator [magnitude polynomial M (x) 8], which utilizes the syndromes obtained serially from the interleaved codes R (x) 1 that are received by the input unit (syndrome generator 3), for determining the coefficients of the error location polynomial L (x) 7 and the coefficients of the error magnitude polynomial M (x) 8,

An output unit (estimator 9) which calculates error signal E (x) 10 and which is combined in summer 11 with delayed raw received input 12 to provide corrected data 13 by employing output data M (x) 8 and L (x) 7 received serially from the processor (polynomial solver 6).

The processing means (polynomial solver 6) employs syndrome polynomial S (x) 5 that has syndromes as coefficients for calculating the coefficients of the error locator polynomial L (x) 7 and the coefficients of the error value polynomial, M (x) 8.

The output means (estimator 9) employs the coefficients of the error locator polynomial L (x) 7, the coefficients of the error value polynomial M (x) 8 and the coded input digital signals (12) to correct errors using Chien search unit 14 which utilizes the error location polynomial L (x) for obtaining an error position polynomial and using Forney's algorithm unit 15 which utilizes the error value polynomial M (x) 8 to determine the error values. With respect to claimed feature of correcting errors using a linear

calculation in a Galois extension field, the RS message block code is viewed as a polynomial and evaluated as a polynomial at some Galois Field element. The Galois Field element at which the polynomial is evaluated is located at one roots of the generator polynomial that are used to create the RS code (also see Abstract and Summary of the Invention).

Cameron does not explicitly disclose the features for entering coded digital signals in parallel and for outputting the obtained digital signals in parallel in accordance with the number of interleaved codes. However, Applicant's own admitted prior art employs a conventional decoder (FIGS. 1 and 5) for decoding Reed-Solomon codes, having an input serial/parallel converter for entering coded digital signals in parallel and an output parallel/serial converter and for outputting the obtained digital signals in parallel. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use well known conventional serial/parallel and parallel/serial converters such as MUX / DEMUX devices, as taught by Applicant's own admitted prior art, in the decoding device of Cameron, which provides the motivation, since the Prior Art deploys Fast and High-Level Error Correction Techniques using the decoding circuit in FIG. 1, which implements a procedure for increasing by a multiple of ten or more the decoding speed of one decoding circuit, and for performing parallel decoding in an error correction process using the Reed-Solomon coding possessing high-level error correction capabilities.

Regarding Claims 3, 8, 14 and 19, Cameron discloses an input unit (syndrome generator 3) for entering coded digital signals from a raw received signal R (x) 1 of

Reed-Solomon (RS) codes Cameron does not explicitly disclose digital signals received in parallel through an i-channel, and the decoding circuit comprises a multiplexer and a demultiplexer, having a ratio of one of i: 1 and 1:i. However, Applicant's own admitted prior art employs a conventional decoder (FIGS. 1 and 5) for receiving Reed-Solomon codes through an i-channel, having an input serial/parallel converter and an output parallel/serial converter such as a well known multiplexer and a demultiplexer respectively for entering coded digital signals in parallel and for outputting digital signals in parallel, respectively, where the channel ratio is (i-mn) and (mn-i). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the Applicant's prior art in the decoding device of Cameron for the same motivational reason as described in the independent claim above.

Regarding Claims 4, 9, 15 and 20, Cameron does not explicitly disclose wavelength division multiplexing of the input digital signals for optical communication transmission. However, Applicant's own admitted prior art describes Error Correction Technique Required by a Fast Optical Communication by computers that employ WDM (Wavelength Division Multiplexing). Further, (FIG. 2) shows the configuration of an error correction circuit that employs a conventional low-speed decoding method for optical communication, which utilizes multiple conventional RS decoders. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the decoding configuration, as taught by Applicant's own admitted prior art, in the decoding device of Cameron, since the decoding method (FIG. 2) achieves the necessary processing speed by an appropriate arrangement of low-speed serial Reed-

Solomon decoders. As the wavelength division multiplexing levels for the optical data communication is increased, cross talk occurs between wavelengths. To cope with the cross talk, FEC (Forward Error Correction) is employed as an error correction method for communication using optical wavelength division multiplexing.

Regarding Claims 5, 10, 16 and 21, Cameron does not explicitly disclose an input unit comprising a sequential circuit and a processor comprising a combinational circuit. However, Applicant's own admitted prior art discloses a decoding circuit (FIG. 1), which employs a processor comprising combinational circuit for the calculation of the coefficients of Err (x), and also for the calculation of the coefficients of the error locator polynomial L (x). He further discloses an input unit comprising a sequential circuit such as an input serial/parallel converter including shift registers. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use combinational circuit, as taught by Applicant's own admitted prior art, in the decoding device of Cameron, thus providing motivation due to higher processing speed and due to the reduction in the number of required arithmetic circuits. And furthermore, since the decoding circuit in FIG. 1 is a combinational circuit that does not require an external controller and registers, in spite of the high processing speed that can be attained, power consumption can be reduced.

Regarding Claims 6, 11 and 17, Cameron discloses a decoder unit (2), which is used for error correction of digital signal (see Abstract and Summary of the Invention).

Conclusion

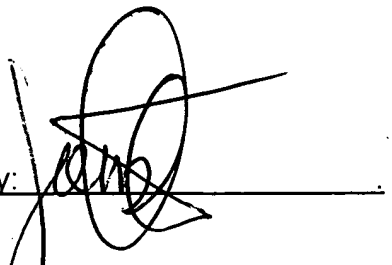
6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 6 August 2004
Office Action: Non-Final Rejection

By: 

James C Kerveros
Examiner
Art Unit 2133

Guy J. Lamarre
Primary Examiner